EE 203 NAME_____
Final Exam
Spring 2006

Instructions: There are 10 questions on this exam that are worth 2 pts each and 8 problems worth 10 points each. Answer all questions and solve all problems. All work should be included on the exam itself. Attach additional sheets only if you run out of space on a problem. Students may bring 8 pages of notes to the exam. Calculators are permitted but can not be shared.

Unless stated to the contrary, assume all diodes are ideal, all MOS transistors are from a process with $\mu_n C_{OX}=100\mu A/V^2$, $\mu_p C_{OX}=33\mu A/V^2$, $V_{Tn}=1V$, $V_{Tp}= -1V$, $\gamma=.5V^{1/2}$,$\lambda=0.1V^{-1}$and all BJT transistors are from a process with $J_S= 10^{-13}A/\mu^2$, $\beta=100$ and $V_{AF} = 200V$ for both npn and pnp transistors. You may neglect γ, λ, and V_{AF} effects if neglecting these effects does not substantially affect the solution of a problem.

Questions:

1. List the design variables for the BJT and for the MOSFET

BJT _____ MOSFET _____

2. What region of operation of the MOSFET corresponds to the Saturation region of the BJT?

3. In the bipolar process described at the top of this exam, what is the ratio of the small signal parameters g_m and g_π at a collector current of 5mA and at a temperature of 300°K?

4. There were two major technical challenges facing amplifier designers prior to the work of Black on feedback and feedback dramatically reduced both of these challenges. What were they?

5 A system has a transfer function $T(s)=\frac{s-5}{s^2+4s+3}$. What are the poles of the transfer function?

6. What is the output impedance of an ideal transconductance amplifier?

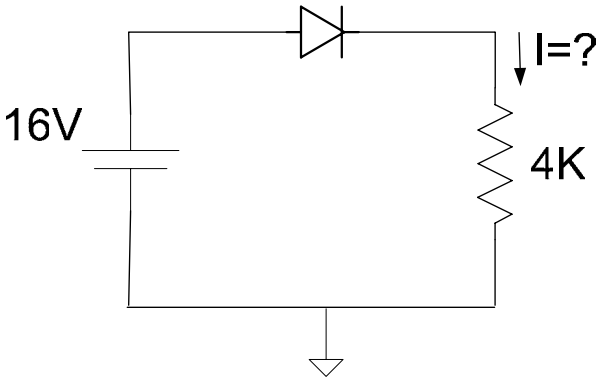
7. In class three types of multivibrators were discussed. One of the three types can be used for a digital memory. Which type is it?

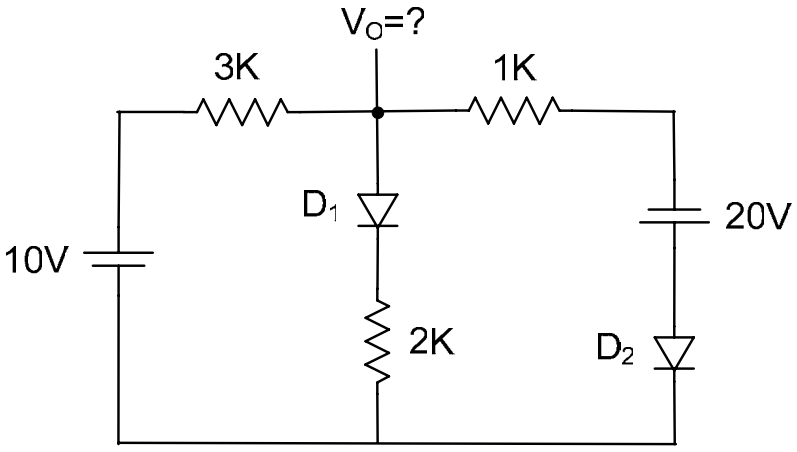
8. There is one major benefit from using NAND gates rather than NOR gates when implementing Boolean Functions in static CMOS logic. What is that benefit and why does this benefit occur?

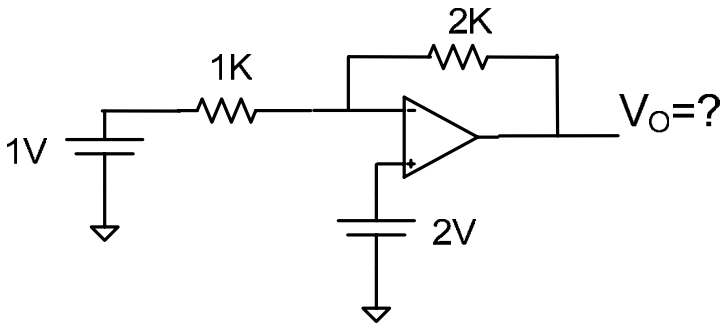
9. What parameter of an operational amplifier characterizes the maximum rate of change in the output voltage?

10. For an excess bias voltage in a MOSFET of 250mV, what is the ratio of the small signal transconductance of a MOSFET to that of a BJT if they are both biased at an output current of 1mA?

Problem 1 Determine the variables indicated with a ? Assume the diodes are ideal.

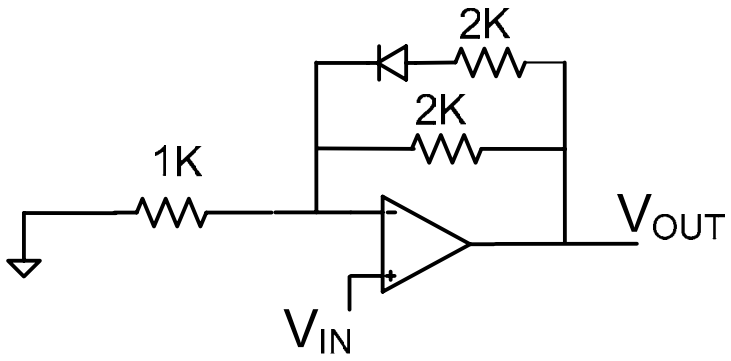


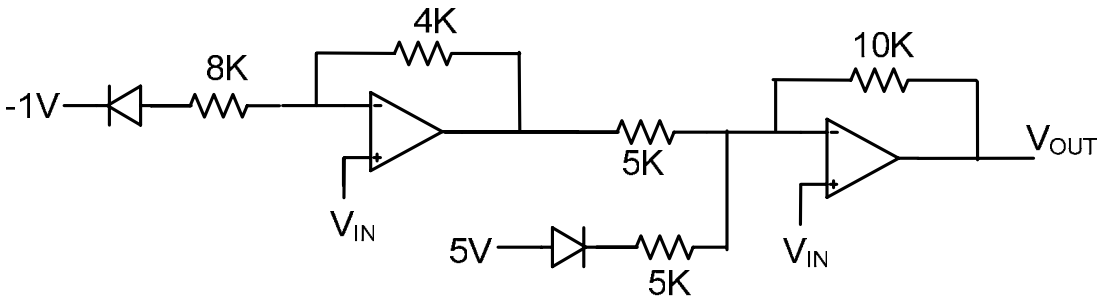




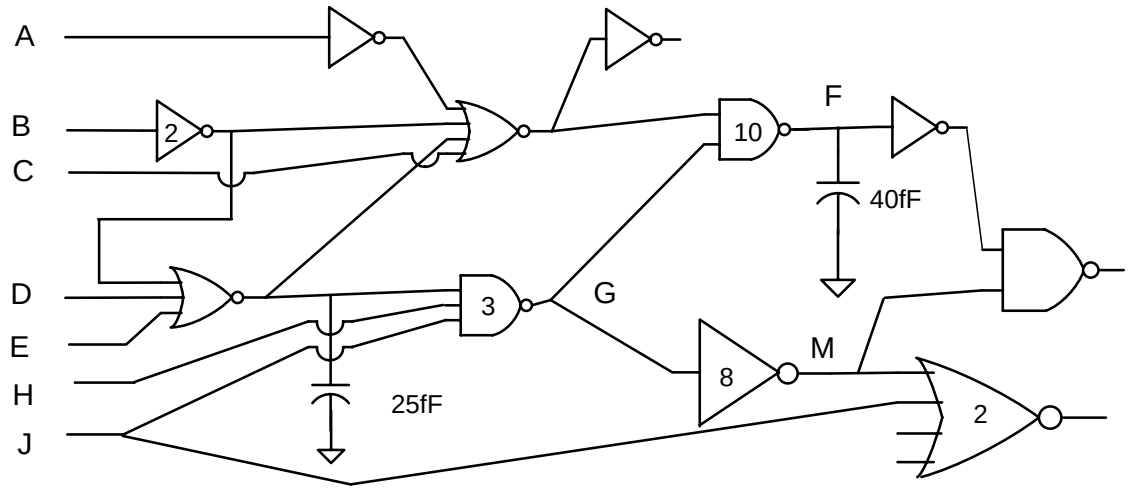
Problem 2

Obtain an expression for and plot the transfer characteristics of the following circuits. Assume the diodes are ideal.





Problem 3 Determine the propagation delay from D to M. Assume all devices are sized for equal worst-case rise and fall time and that the overdrive of the gates, if different than 1, are as indicated. Assume you are working in a process wit V_{DD}=5V, V_{TN}=1V, V_{TP}=-1V, u_nC_{OX}=100uA/V^2, C_{OX}=4fF/u^2, Lmin = 0.25μ,Wmin = 0.25μ and μ_n/μ_p=3..



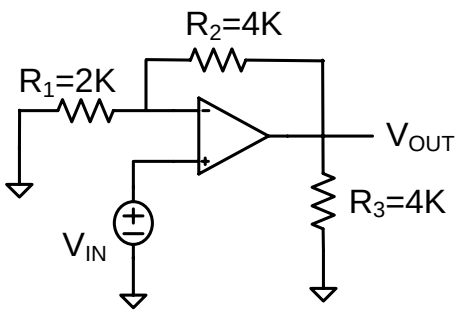
Problem 4

Design Boolean circuits that will implement the function $F = A\overline{B}C + B\overline{C} + \overline{A}B$ with

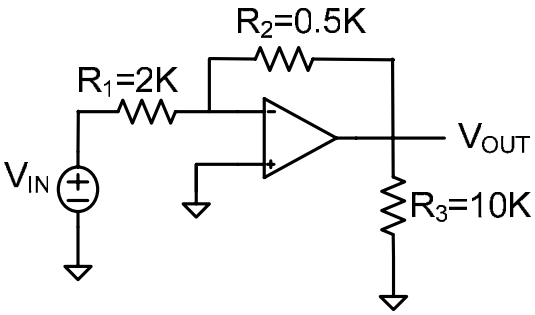
a) Static CMOS (at the gate level using only NAND,NOR and INV gates)
b) Complex Logic Gates (at the transistor level)
c) Pass Transistor Logic (at the transistor level)
d) Dynamic Logic (at the transistor level)

Assume the input variables A,B and C are available and that if compliments of variables are needed, generate them with Static CMOS inverters. You need not size the transistors.

Problem 5 Determine the 3dB bandwidth of the following three systems. Unless stated to the contrary, assume that the GB of the op amps is 3MHz.



(a)



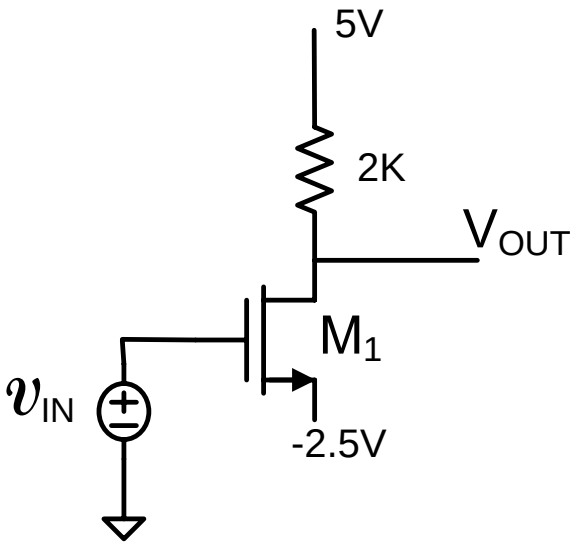
(b)

$$T(s) = 40\frac{s+1}{s+4}$$

(c)

Problem 6 Assume the input signal v_{IN} is a small signal source and that the length of M_1 is 10μ

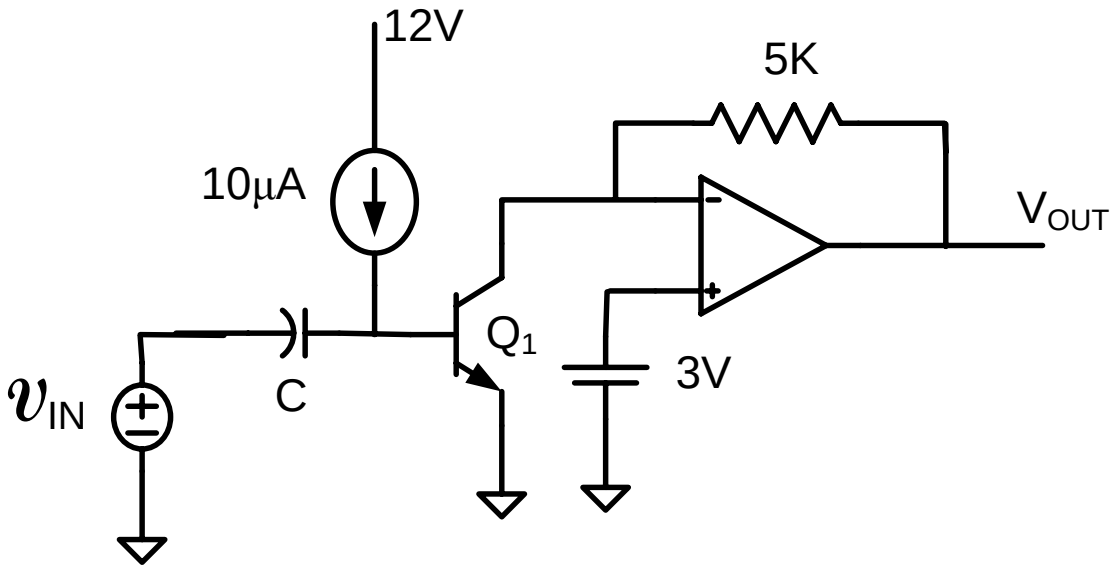
a) Determine the width W_1 of the transistor so that the quiescent output voltage is 3V when v_{IN}=0V.
b) Determine the transconductance gain, g_m, for M_1 at the Q-point determined in part a)
c) Determine the small signal voltage gain at the Q-point determined in part a)



Problem 7 Assume the capacitor C is large.

a) Determine the quiescent output voltage.

b) Determine the steady state output voltage if the small signal input is $v_{IN}(t)=.001\sin 5000t$



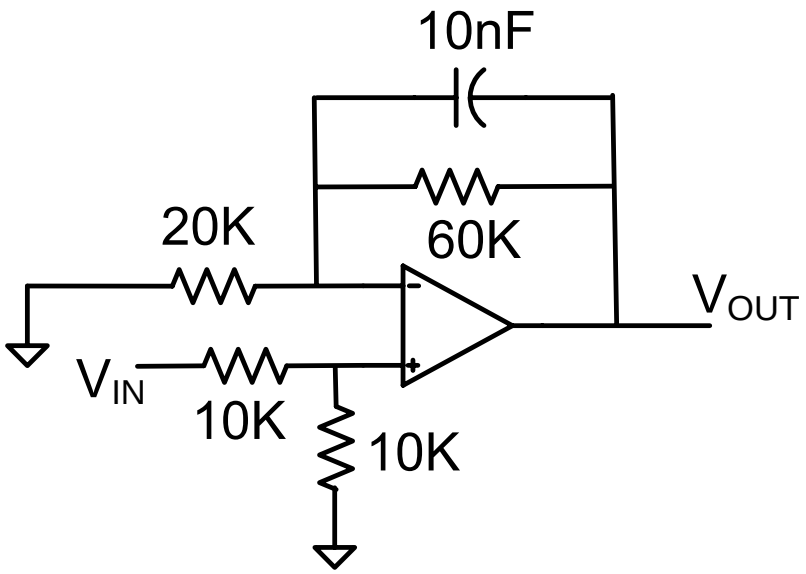
Problem 8 For the circuit shown

a) Obtain an expression for the transfer function.

b) Plot the magnitude of the transfer function

c) Determine the steady state response if $V_{IN}(t) = 0.5\sin(2000t + 60°)$

Assume the op amp is ideal.



(This page does not contain an additional problem. Process information from first page is repeated at request of students.)

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